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(See notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office
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1. Your reference — PHGB020170

2. Patent application number *(The Patent Office will fill in this part)* — 0223034.0 — 04 OCT 2002

3. Full name, address and postcode of the or of each applicant *(underline all surnames)* — KONINKLIJKE PHILIPS ELECTRONICS N.V.
GROENEWOUDSEWEG 1
5621 BA EINDHOVEN
THE NETHERLANDS

Patents ADP Number *(if you know it)* — 7419294001

If the applicant is a corporate body, give the country/state of its incorporation — THE NETHERLANDS

4. Title of the invention — POWER SEMICONDUCTOR DEVICES

5. Name of your agent *(if you have one)*
"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)* — Daniel SHARROCK
Philips Intellectual Property and Standards
Cross Oak Lane
Redhill
Surrey RH1 5HA

Patents ADP number *(if you know it)* — 8359658001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority Application number *(if you know it)*	Date of filing *(day/month/year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day/month/year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer "Yes" if:*
   a) any applicant named in part 3 is not an inventor, or
   b) there is an inventor who is not named as an applicant, or
   c) any named applicant is a corporate body.
   See note (d)) — YES

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Patents Form 1/77

9. Enter the number of sheets for any of the following items you are filing with this form.
Do not count copies of the same document.

Continuation sheets of this form	
Description	5
Claims(s)	0
Abstract	0
Drawings	3

10. If you are also filing any of the following, state how many against each item:

Priority Documents

Translations of priority documents

Statement of inventorship and right to grant of a patent (*Patents Form 7/77*)

Request for preliminary examination and search (*Patents Form 9/77*)

Request for substantive examination (*Patents Form 10/77*)

Any other documents (*Please specify*)

11. I/We request the grant of a patent on the basis of this application.

Signature D. J. [illegible] Date 4 OCT 2002

12. Name and daytime telephone number of person to contact in the United Kingdom 01293 815399 (Daniel Sharrock)

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Notes

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d) *If you have answered "Yes" Patents Form 7/77 will need to be filed.*

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DESCRIPTION

POWER SEMICONDUCTOR DEVICES

The present invention relates to power semiconductor devices, and more particularly to insulated gate field effect power transistors (commonly termed "MOSFETs").

Lateral double-diffused metal-oxide-semiconductor (commonly termed "DMOS" devices) are well known in the art. A typical DMOS structure is described for example on pages 336 to 339 of "Power Semiconductor Devices" by B. Jayant Baliga. The contents of these pages are hereby incorporated herein as reference material. Such a DMOS structure comprises a semiconductor body having a drain drift region overlying a more heavily doped drain contact region, each of the same, first conductivity type. The drain contact region is contacted by a drain electrode at the bottom major surface of the semiconductor body. A source region of the first conductivity type and a channel-accommodating region of a second, opposite conductivity type are provided adjoining the top major surface of the semiconductor body. A portion of the drain drift region also adjoins the top major surface. An insulating layer is provided on the top major surface which at least covers a portion of the channel-accommodating region lying between the source and drain drift regions, and a gate electrode is provided over the insulating layer.

In many power switching applications, for example the high side FET (ControlFET) in voltage regulation module (commonly termed "VRM") applications, it is very important to reduce power losses from the FET that arise from switching and conduction.

It is an object of the present invention to provide a DMOS transistor which exhibits reduced power losses.

Various novel concepts, inventive concepts and specific embodiments of the invention are disclosed herein, particularly, but not exclusively with reference to Figures 4 to 9 of the accompanying Drawings.

In accordance with one embodiment of the invention, a DMOS transistor includes a trench in the semiconductor body of the device below the insulated gate electrode, and an insulated electrode in the trench which extends from adjacent the gate electrode, alongside and/or through the channel-accommodating region, to the drain drift region. The trench electrode is arranged for connection to a bias potential.

Prior art structures and embodiments of the invention will now be described by way of example and with reference to the accompanying schematic drawings, wherein:

Figure 1 shows simulated turn-on waveforms for gate voltage, drain voltage and switching power loss plotted as a function of time for a known DMOS device. Also shown is the total actual switching loss period for DMOS technology;

Figure 2 shows a 7um cell DMOS technology cell employed in simulations described herein;

Figure 3 shows a typical trench technology cell;

Figure 4 shows simulated turn-on switching waveforms comparing the known DMOS device of Figure 2 and a structure embodying the invention having the same (9mΩ) on-state resistance;

Figure 5 shows simulated turn-on switching power losses plotted as a function of time comparing a known DMOS device and a structure embodying the invention having the same (9mΩ) on-state resistance;

Figure 6 shows simulated 'Miller' feedback capacitance (Cgd) plotted as a function of drain-source voltage (Vds) comparing a known DMOS device and a structure embodying the invention;

Figure 7 shows simulated specific on-state resistance plotted as a function of gate voltage, comparing a known DMOS device and a structure embodying the invention;

Figure 8 shows a cell according to an embodiment of the invention; and

Figure 9 shows simulated drain current plotted as a function of drain voltage for a known DMOS device and a structure embodying the invention.

It should be noted that Figures 2, 3 and 8 are diagrammatic and not drawn to scale. Relative dimensions and proportions of parts of these Figures have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the Drawings.

For FETs used in power switching applications, a "figure of merit" has been developed that describes the power losses associated with the FET. This figure of merit is obtained by multiplying the on-state resistance by the Miller gate-drain charge (Qgd) of the device. However, this figure of merit only accounts for the switching losses that occur during the gate plateau period. The actual switching loss must also include the contribution to switching losses that occurs due to the rate of change of the drain voltage at turn on (figure 1) and turn off. When DMOS technology (figure 2) is compared to trench technology (figure3) for the same on-state resistance, it is known that DMOS technologies generally exhibit quicker switching and lower switching losses. This is generally true even though the figure of merit (Rdson x Qgd) for the DMOS technology may be higher than that for trench technology. What makes DMOS technology more attractive than trench technology as a switching platform is its inherent geometry (figure 2). The benefit of DMOS technology is that the depletion width below the gate electrode is much wider. The structure is such that the body junctions force the depletion under the gate electrode to reach further. Therefore, the depletion associated with Cgd at high drain voltage is wide and since Cgd is inversely proportional to the depletion width than that component of Cgd is lower. This contributes to a rapid fall in Vds as the device turns on because dV/dt=Ig/Cgd where Ig is constant (figure 6).

An alternative way to visualise this is to consider the "divD" effect. That is, the equipotentials are such that they "direct" the discharge current into the body rather than capacitively into the gate electrode. This means for a given rate of dV/dt the proportion of discharge current going into the gate electrode becomes smaller and for a given gate current the dV/dt is faster. Thus the discharging current component of Cgd is reduced. Unfortunately, DMOS

technology for a given on-state resistance is significantly more expensive than trench technology due to the much higher specific on state resistance (figure 7) and trench technology dominates the market for this type of product.

Thus, the figure of merit (Rdson x Qgd) normally given to describe the high side FET may not be an accurate measure when switching losses are compared for different technologies. The present inventors have devised a cell structure that couples trench technology specific on-state resistance with DMOS technology switching performance. The structure described herein achieves that requirement. An exemplary embodiment is shown in Figure 8. The structure illustrated includes a gate electrode and an insulated electrode in a trench below the gate electrode. Each electrode may be formed of polysilicon, for example. The electrode bounded within the trench is isolated from the gate electrode, which has been masked to overlap the trenched electrode.

The trenched electrode is biased independently of the gate electrode to say the VRM load voltage for example (the VRM load voltage may typically be 12v). Until such time as a gate potential is applied to the upper electrode no channel is formed between source and drain. Once a gate voltage has been applied to the upper electrode, which is above that of the threshold level of the device a channel is formed and the device operates in the normal way. However, the upper gate electrode has been shielded by the trench bound electrode being held at the 12v load voltage.

A 4μm cell pitch hybrid structure has been simulated and compared with the best performance currently offered by a commercially available DMOS structure (7μm pitch) having an on-state resistance of 9mΩ. Simulation demonstrates that the hybrid structure exhibits Cgd that is >3 orders of magnitude lower than that of the DMOS structure for a 12v drain voltage. Thus the hybrid structure exhibits very high dV/dt (figure 4), a gate-drain charge of ~1nC (figure 4), a figure of merit of ~9mΩ.nC, a 40v breakdown voltage (figure 9) and an overall switching loss, which is only ~60% of that simulated for DMOS technology (figure 5).

From reading the above disclosure, other modifications and variations will be apparent to persons skilled in the art. Such modifications and variations may involve other features which are already known in the art and which may be used instead of or in addition to features already disclosed herein. No specific patent claims have yet been formulated in this application to particular combinations of features, and it should be understood that the scope of the disclosure of the present application includes any and every novel feature or combination of features disclosed herein either explicitly or implicitly and together with all such modifications and variations, whether or not relating to the main inventive concepts disclosed herein and whether or not it mitigates any or all of the same technical problems as the main inventive concepts. The applicants hereby give notice that patent claims may be formulated to such features and/or combinations of such features during prosecution of the present application or of any further application derived or claiming priority therefrom.

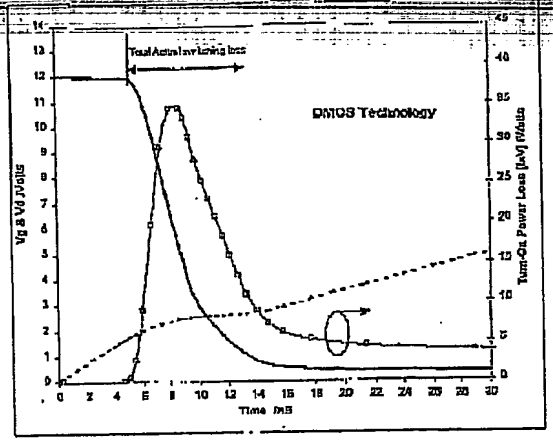


Fig. 1

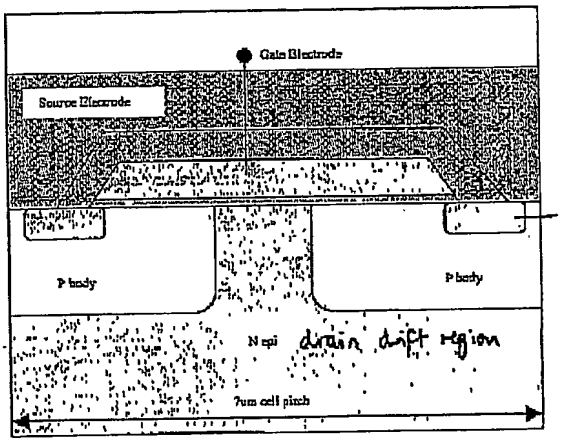


Fig. 2

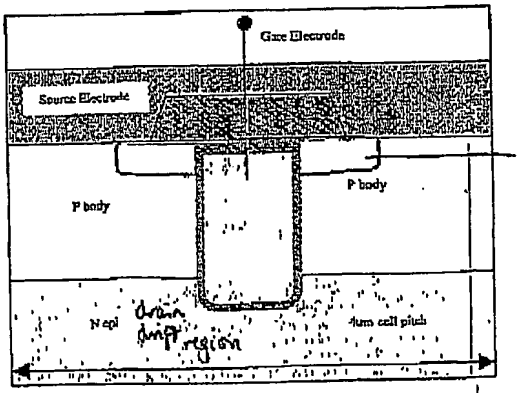


Fig. 3

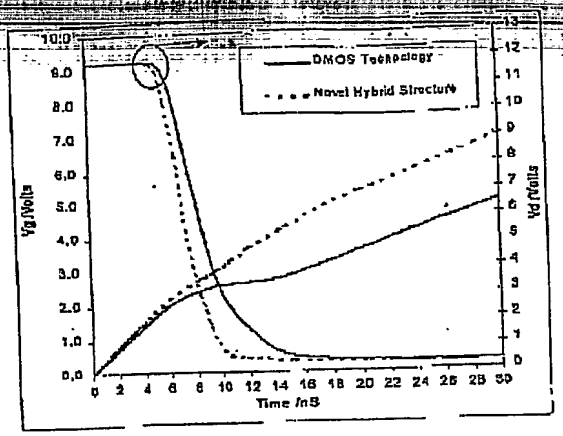


Fig.4

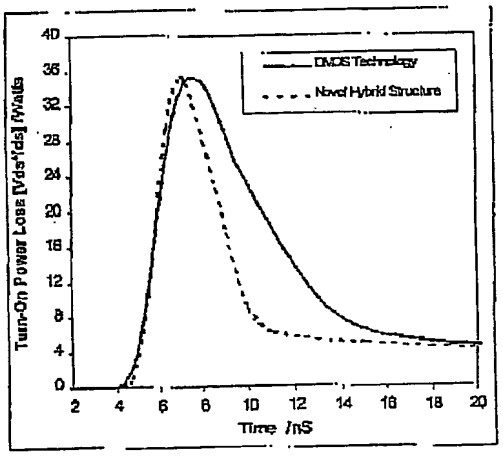


Fig.5

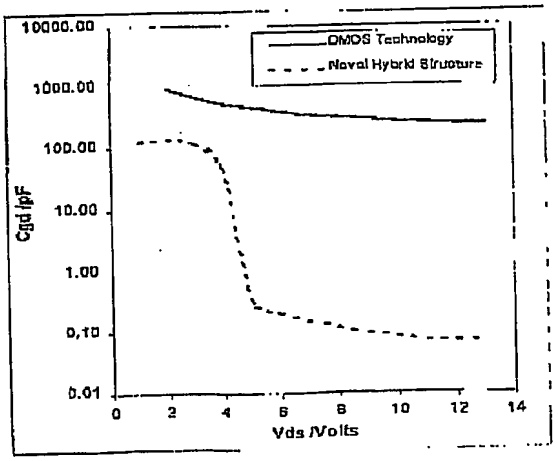


Fig.6

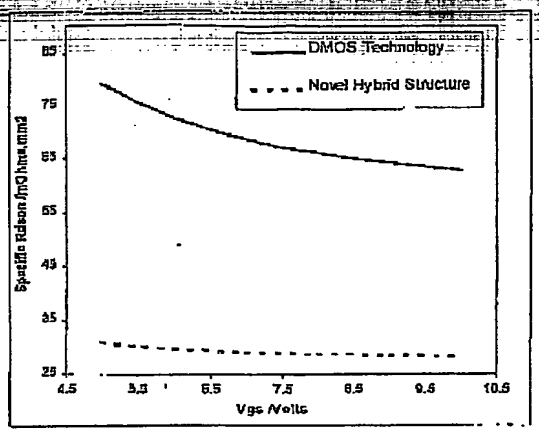
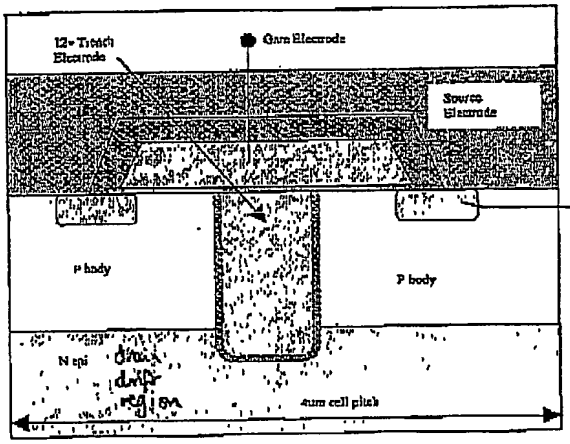


Fig. 7



source region

Fig. 8

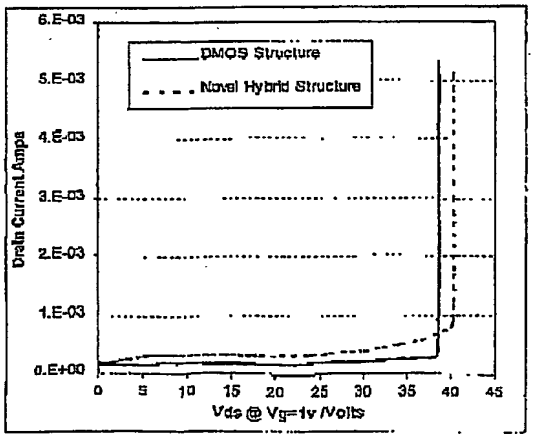


Fig. 9